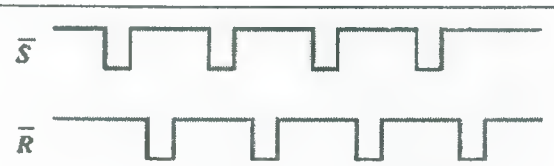
Al-Mansoura University
Faculty of Engineering
Communications and Elect. Dept

Logic Circuits 2
2nd year Students
Time 3 Hours

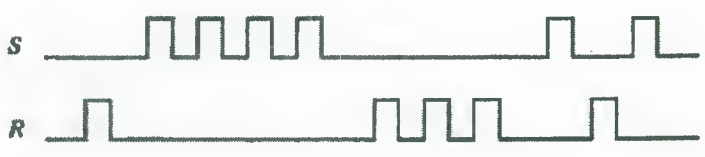
Attempt in all questions and assume any missing data.

Q1:(a)-If the waveforms in Figure (1) are applied to an active-low input S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts low.

(b)- Repeat (a) for the input waveforms in Figure 2 applied to an active-high S-R latch.



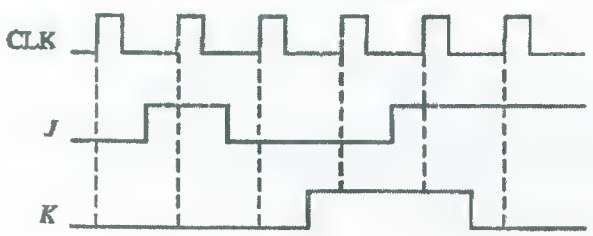
Figure(1)



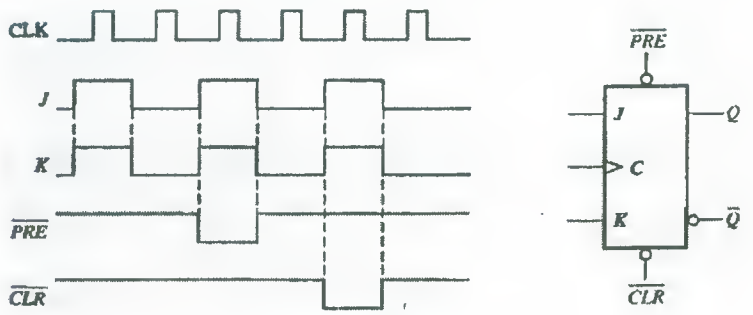
Figure(2)

Q2:(a)-For a positive edge-triggered J-K flip-flop with inputs as shown in Figure(3), determine the Q output relative to the clock. Assume that Q starts low.

(b)- Determine the Q waveform relative to the clock if the signals shown in Figure(4) are applied to the inputs of the J-K flip-flop. Assume that Q is initially low.



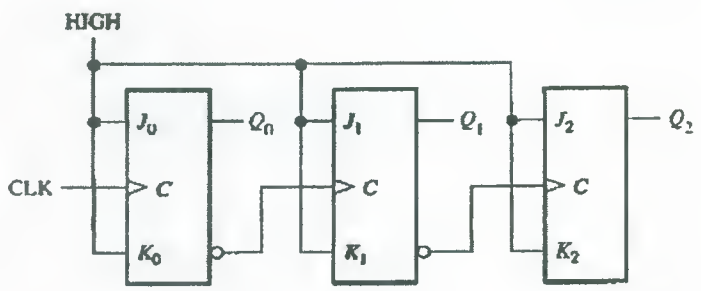
Figure(3)



Figure(4)

Q3:(a)- For the ripple counter in Figure(5), show the complete timing diagram for ten clock pulses. Show the clock, Q_0, Q_1 and Q_2 waveforms.

(b)-Design a 4-bit synchronous binary counter and draw the timing diagram for the output signals.



Figure(5)

Q4:(a)-Design a 4-bit synchronous decade counter (BCD) and draw its timing diagram.

(b)-Explain with drawing a 4-bit binary up/down counter and develop the Q output waveforms for this counter.

Q5:(a)- Design a 4-bit serial in/parallel output shift register. Show the states of the 4-bit serial in/parallel out shift register for the data input and clock waveforms in Figure(6). The register initially contains all 1s.

Figure(6)

(b)- Explain with drawing a 4-bit parallel in/serial out shift register using the logic gates AND, OR, NOT, and using the D type positive edge triggered flip-flop. The control line Shift/Load is used to control the shift/load process of the register. To synchronize the operations of the register the clock signal must be used.

Q6:(a)- Design and explain a logic circuit diagram of the serial-to-parallel converter which convert the data packet shown in Figure (7) to parallel form.

Figure (7)

(b)- A bidirectional shift register is one in which the data can be shifted either left or right. It can be implemented by using gating logic that enables the transfer of a data bit from one stage to the next stage to the right or to the left depending on the level of a control line. Design a 4-bit bidirectional shift register and explain its operation.

Q7:(a)- Draw the block diagram of a 3-dimensional RAM memory showing address bus, address decoders, bidirectional data bus, and read/write inputs. Explain the function of each component.

(b)-Design an SRAM memory with the following specifications:

(1)-Memory capacity is 128 rows x 256 columns x 8 bit.

(2)-The control signal lines are $\overline{CS}$, $\overline{WE}$, $\overline{OE}$.

(3)-Bidirectional data buses are used.

Q8:(a)-Explain with drawing the following basic operation of the DRAM:

(1)-Writing a 1 into the memory cell. (2) Writing a 0 to memory cell.

(3)-Reading a 1 from the memory cell. (4)- Refreshing a stored 1.

(b)-Explain with drawing the following basic operation of the flash memory cell:

(1)-The programming of 0 and 1 in a flash cell.

(2)-The read operation of 0 and 1.

(3)-The processes of removing charge from a cell during erase.